CLAIMS

What is claimed is:

1. A printed circuit board comprising:

a substrate having at least one electrically insulative layer; and

at least two conductive trace layers formed on opposing sides of the at least one electrically insulative layer, wherein at least one of the at least two ~~conductive~~ layers includes at least two signal traces and at least one voltage reference trace, the conductive traces being configured such that at least one voltage reference trace is between each two signal traces.

2. The printed circuit board of claim 1, wherein at least one ~~conductive~~ trace includes at least one direction change in its length over the at least one electrically insulative layer.

3. The printed circuit board of claim 1, wherein the at least one electrically insulative layer comprises a plurality of insulative layers, each separated by at least one conductive trace layer.

4. The printed circuit board of claim 1, wherein at least one of the conductive trace layers is a voltage reference plane.

5. The printed circuit board of claim 4, wherein the at least one voltage reference trace is coupled to the voltage reference plane.

6. The printed circuit board of claim 1, further comprising a passivation layer deposited on at least one of the conductive trace layers.

7. The printed circuit board of claim 1, wherein the at least one electrically insulative layer ~~is~~ comprises two electrically insulative layers separated by a conductive layer, and wherein the at least one voltage reference trace is electrically coupled to the conductive layer.

8. The printed circuit board of claim 1, wherein at least one of the at least two conductive trace layers further comprises at least one voltage reference bus, wherein the at least one voltage reference trace is electrically coupled to the at least one voltage reference bus.

9. The printed circuit board of claim 1, wherein at least a portion of the ~~conductive~~ traces are embodied as vias.

10. A printed circuit board comprising at least one electrically insulative layer and at least one electrically conductive layer, the at least one electrically conductive layer comprising at least one signal trace electrically isolated from a voltage reference portion thereof, wherein the voltage reference portion has a greater surface area than the at least one signal trace.

11. The printed circuit board of claim 10, wherein a majority of the at least one electrically conductive layer is comprised in the voltage reference portion.

12. The printed circuit board of claim 10, wherein the voltage reference portion comprises a voltage reference bus having voltage reference traces extending therefrom.

13. An electronic device comprising:

at least one electrically insulative layer; and

at least one conductive layer, the conductive layer comprising a voltage reference bus having at least one voltage reference trace extending therefrom and at least two signal traces electrically isolated from the at least one voltage reference trace, wherein the at least one voltage reference trace and at least two signal traces are configured such that each signal trace is separated from each other signal trace by at least one voltage reference trace.

14. The electronic device of claim 13, further comprising a passivation layer deposited on ~~at least one of~~ the at least one conductive layer.

15. A printed circuit board comprising:

at least one voltage reference plane substantially coextensive with a portion of a substrate; and

at least one signal trace substantially co-planar with the voltage reference plane and electrically isolated therefrom, the voltage reference plane having a substantially greater surface area than any one signal trace.

16. The printed circuit board of claim 15, wherein the at least one signal trace is electrically isolated from the at least one voltage reference plane by at least one trough.

17. The printed circuit board of claim 15, further comprising a passivation layer deposited on the at least one signal trace and the at least one electrically insulative layer.

18. The printed circuit board of claim 15, wherein the at least one voltage reference plane is a substantially continuous voltage reference plane.

19. A printed circuit board comprising at least one voltage reference plane having at least one ~~co-planar~~ coplanar signal trace isolated therefrom, wherein the at least one voltage reference plane includes a surface area greater than any one signal trace.

20. An electronic system comprising:

a processor;

a memory device associated with the processor; and

at least one of an input device, an output device and a data storage device associated with the processor;

wherein at least one component of the electronic system comprises at least two conductive trace layers formed on opposing sides of at least one electrically insulative layer, wherein each of the at least two conductive trace layers includes at least two signal traces and at least one voltage reference trace, the ~~conductive~~ traces being configured such that at least one voltage reference trace is between each of the two signal traces.

21. The electronic system of claim 20, wherein at least one of the at least two signal traces includes at least one non-linear path in its extent over the at least one electrically insulative layer.

22. An electronic system comprising:

a processor;

a memory device associated with the processor; and

at least one of an input device, an output device and a data storage device associated with the processor;

wherein at least one component of the electronic system comprises a voltage reference plane substantially coextensive with a portion of a substrate and at least one signal trace substantially ~~co-planar~~ coplanar with and electrically isolated from the voltage reference plane, the voltage reference plane having a surface area greater than the at least one signal trace.